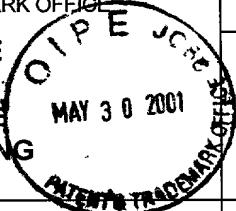
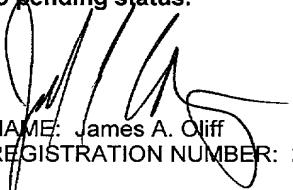


(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT & TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER 109681
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		
 INTERNATIONAL APPLICATION NO. PCT/JP00/06767		U.S. APPLICATION NO. (if known, sec 37 C.F.R.1.5) 09/856924
INTERNATIONAL FILING DATE September 29, 2000		PRIORITY DATE CLAIMED October 4, 1999
TITLE OF INVENTION SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT		
APPLICANT(S) FOR DO/EO/US Nobuaki HASHIMOTO		
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:		
1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.		
2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.		
3. <input checked="" type="checkbox"/> This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).		
4. <input type="checkbox"/> A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.		
5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2)) <ul style="list-style-type: none"> a. <input type="checkbox"/> is transmitted herewith (required only if not transmitted by the International Bureau). b. <input checked="" type="checkbox"/> has been transmitted by the International Bureau. c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US) 		
6. <input checked="" type="checkbox"/> A translation of the International Application into English (35 U.S.C. 371(c)(2)).		
7. <input type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)) <ul style="list-style-type: none"> a. <input type="checkbox"/> are transmitted herewith (required only if not transmitted by the International Bureau). b. <input type="checkbox"/> have been transmitted by the International Bureau. c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired. d. <input type="checkbox"/> have not been made and will not be made. 		
8. <input type="checkbox"/> A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).		
9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).		
10. <input type="checkbox"/> A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).		
Items 11. to 16. below concern other document(s) or information included:		
11. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98.		
12. <input checked="" type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.		
13. <input checked="" type="checkbox"/> A FIRST preliminary amendment.		
<input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment.		
14. <input type="checkbox"/> A substitute specification.		
15. <input type="checkbox"/> Entitlement to small entity status is hereby asserted.		
16. <input type="checkbox"/> Other items or information:		

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 097858924	INTERNATIONAL APPLICATION NO. PCT/JP00/06767	ATTORNEY'S DOCKET NUMBER 109681	
17. <input checked="" type="checkbox"/> The following fees are submitted:		CALCULATIONS	PTO USE ONLY
Basic National fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO \$860.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) \$690.00 No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) \$710.00 Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$1,000.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) \$ 100.00			
ENTER APPROPRIATE BASIC FEE AMOUNT =		\$860.00	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input checked="" type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).		\$	
<input checked="" type="checkbox"/> Claims Number Filed Number Extra Rate Total Claims 32 - 20 = 12 X \$ 18.00 \$216.00			
<input checked="" type="checkbox"/> Independent Claims 2 - 3 = 0 X \$ 80.00 \$			
<input checked="" type="checkbox"/> Multiple dependent claim(s)(if applicable) + \$270.00 \$			
TOTAL OF ABOVE CALCULATIONS =		\$1076.00	
<input checked="" type="checkbox"/> Reduction by 1/2 for filing by small entity, if applicable. - \$			
SUBTOTAL =		\$1076.00	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input checked="" type="checkbox"/> 30 month from the earliest claimed priority date (37 CFR 1.492(f)). +		\$	
TOTAL NATIONAL FEE =		\$1076.00	
		Amount to be refunded	\$
		Charged	\$
a. <input checked="" type="checkbox"/> Check No. <u>119461</u> in the amount of <u>\$1076.00</u> to cover the above fees is enclosed. b. <input type="checkbox"/> Please charge my Deposit Account No. _____ in the amount of \$_____ to cover the above fees. A duplicate copy of this sheet is enclosed. c. <input checked="" type="checkbox"/> The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. <u>15-0461</u> . A duplicate copy of this sheet is enclosed.			
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.			
SEND ALL CORRESPONDENCE TO: OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320			
 NAME: James A. Olioff REGISTRATION NUMBER: 27,075			
 NAME: Joel S. Armstrong REGISTRATION NUMBER: 36,430			

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Application No.: US National Stage of PCT/JP00/06767

Filed: May 30, 2001

Docket No.: 109681

For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME,
CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claims 7, 10, 17-19, 27 and 29 as follows:

7. (Amended) The semiconductor device as defined in claim 1,

wherein a recognition hole is formed in the substrate at a position differing from the
holes; and

wherein a recognition pattern is formed over the recognition hole on the side of a
surface of the substrate including the interconnecting pattern.

10. (Amended) The semiconductor device as defined in claim 1,

wherein the conductive members are a plurality of layered bumps.

17. (Amended) The semiconductor device as defined in claim 1,

wherein the semiconductor chip is mounted face-down to the substrate.

18. (Amended) A circuit board over which is mounted the semiconductor device
as defined in claim 1.

19. (Amended) An electronic instrument provided with the semiconductor device as defined in claim 1.

27. (Amended) The method of fabricating a semiconductor device as defined in claim 20, further comprising

a step of forming a recognition hole in the substrate at a position differing from the holes, and forming a recognition pattern over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

29. (Amended) The method of fabricating a semiconductor device as defined in claim 20,

wherein the conductive members are a plurality of layered bumps.

REMARKS

Claims 1-32 are pending. By this Preliminary Amendment, claims 7, 10, 17-19, 27 and 29 are amended to eliminate multiple dependencies. Prompt and favorable consideration on the merits is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. 1.121(c)(1)(ii)).

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Joel S. Armstrong
Registration No. 36,430

JAO:JSA/zmc
Attached: APPENDIX
Date: May 30, 2001

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

<p>DEPOSIT ACCOUNT USE AUTHORIZATION Please grant any extension necessary for entry; Charge any fee due to our Deposit Account No. 15-0461</p>
--

APPENDIX

Changes to Claims:

The following are marked-up versions of the amended claims:

7. (Amended) The semiconductor device as defined in ~~claim 1 any one of claims~~

~~1 to 6,~~

wherein a recognition hole is formed in the substrate at a position differing from the holes; and

wherein a recognition pattern is formed over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

10. (Amended) The semiconductor device as defined in ~~claim 1 any one of claims~~

~~1 to 6,~~

wherein the conductive members are a plurality of layered bumps.

17. (Amended) The semiconductor device as defined in ~~claim 1 any one of claims~~

~~1 to 6,~~

wherein the semiconductor chip is mounted face-down to the substrate.

18. (Amended) A circuit board over which is mounted the semiconductor device as defined in ~~claim 1 any one of claims 1 to 6.~~

19. (Amended) An electronic instrument provided with the semiconductor device as defined in ~~claim 1 any one of claims 1 to 6.~~

27. (Amended) The method of fabricating a semiconductor device as defined in ~~claim 20 any one of claims 20 to 26,~~ further comprising

a step of forming a recognition hole in the substrate at a position differing from the holes, and forming a recognition pattern over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

29. (Amended) The method of fabricating a semiconductor device as defined in claim 20~~any one of claims 20 to 26~~,
wherein the conductive members are a plurality of layered bumps.

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME,
CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

TECHNICAL FIELD

5 The present invention relates to a semiconductor device and a method of fabricating the semiconductor device, a circuit board, and an electronic instrument.

BACKGROUND ART

As one type of CSP (Chip Scale/Size Package) semiconductor devices, a semiconductor device with a structure in which a semiconductor chip is mounted face-down to a substrate has been known. In such a face down structure, a semiconductor chip is generally mounted on a surface of the substrate on which an interconnecting pattern is formed. Therefore, since part of the interconnecting pattern is covered with the semiconductor chip, the degree of freedom in designing the interconnecting pattern is limited.

20 DISCLOSURE OF THE INVENTION

The present invention has been achieved to solve this problem. An objective of the present invention is to provide a semiconductor device and a method of fabricating the same capable of increasing the degree of freedom in designing an 25 interconnecting pattern without decreasing connection reliability, a circuit board, and an electronic instrument.

(1) According to the present invention, there is provided

a semiconductor device comprising:

a substrate including a plurality of holes and a surface over which an interconnecting pattern is formed, part of the interconnecting pattern extending over the holes;

5 a semiconductor chip disposed over another surface of the substrate and including a plurality of electrodes to be positioned over the holes; and

10 conductive members provided within the holes for electrically connecting the electrodes to the interconnecting pattern.

15 According to the present invention, the conductive members formed on the electrodes of the semiconductor chip are disposed within the holes and connected to the interconnecting pattern. Therefore, the interconnecting pattern is located on the side of the substrate opposite to the mounting region of the semiconductor chip. Specifically, since the interconnecting pattern is not covered with the semiconductor chip, the interconnecting pattern can be designed without limitation. Moreover, there is a substrate between the 20 interconnecting pattern and the semiconductor chip. Therefore, signals in an integrated circuit in the semiconductor chip scarcely interfere with signals in the interconnecting pattern, whereby cross talk can be reduced. Because of this, a semiconductor device with an increased degree of freedom in 25 designing the interconnecting pattern can be obtained without decreasing connection reliability.

(2) In this semiconductor device, a resin may be provided

between the substrate and the semiconductor chip.

According to this semiconductor device, the semiconductor chip is mounted on a surface of the substrate on which the interconnecting pattern is not required, and a resin is provided between the substrate and the semiconductor chip. Therefore, if an interconnecting pattern is not formed over the surface of the substrate over which the semiconductor chip is mounted, the resin is provided on the substrate exhibiting comparatively excellent adhesion, so that delamination can be reduced. Because of this, a semiconductor device with an increased degree of freedom in designing the interconnecting pattern can be obtained more effectively without decreasing connection reliability.

(3) In this semiconductor device, the resin may be an anisotropic conductive material containing conductive particles; and the conductive members may be electrically connected to the interconnecting pattern through the conductive particles.

(4) In this semiconductor device, part of the interconnecting pattern may close the holes.

(5) In this semiconductor device, the interconnecting pattern may include a plurality of interconnecting lines; and two or more interconnecting lines may extend over each of the holes.

This enables holes necessary for the substrate can be easily formed.

(6) In this semiconductor device, the other surface of

the substrate may be roughed.

Since a contact area between the resin and the substrate is increased, adhesion between them can be further improved.

5 (7) In this semiconductor device, a recognition hole may be formed in the substrate at a position differing from the holes; and

a recognition pattern may be formed over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

This enables to mount the semiconductor chip easily over the substrate.

(8) In this semiconductor device, the recognition hole may be formed in the substrate outside a mounting region for the semiconductor chip.

This makes it possible to mount the semiconductor chip easily over the substrate.

(9) In this semiconductor device, the recognition pattern may includes:

20 a first pattern extending in the X-axis direction of the two-dimensional coordinate system established on a surface of the substrate; and

a second pattern extending in the Y-axis direction.

This enables the semiconductor chip to be accurately mounted at a given position on the substrate by recognizing the 25 first and second patterns.

(10) In this semiconductor device, the conductive members may be a plurality of layered bumps.

This enables the conductive members to be formed by using existing techniques and devices, for example.

(11) In this semiconductor device, the bumps may include first bumps formed on the electrodes and second bumps formed 5 on the first bumps.

Note that the first and second bumps refer to two arbitrary bumps, and this is applicable to two or more bumps.

(12) In this semiconductor device, at least the first bumps may be ball bumps.

According to this semiconductor device, the first bumps may be formed by the ball bump method. Since existing wire bonder devices can be utilized, the semiconductor device can be fabricated with reduced equipment investment.

(13) In this semiconductor device, the second bumps may be formed of a metal which has a melting point lower than the melting point of the first bumps.

According to this semiconductor device, since the first bumps formed in advance have a higher melting point, the first bumps are less affected by heat for forming the second bumps, 20 for example. Therefore, a plurality of bumps can be easily layered.

(14) In this semiconductor device, the first bumps may be formed of gold.

Gold has a comparatively high melting point.

25 (15) In this semiconductor device, the second bumps may be formed of solder.

(16) In this semiconductor device, the first bumps and

the second bumps may be formed of the same material.

This enables the second bump to also be formed by the ball bump method, for example.

5 (17) In this semiconductor device, the semiconductor chip may be mounted face-down to the substrate.

According to this semiconductor device, the interval between the semiconductor chip and the substrate is increased by the height of the first and second bumps formed on the electrodes of the semiconductor chip, so a large amount of resin can be provided right under the semiconductor chip, thereby enabling the resin to fully function as a stress relaxation layer. If the first bump is formed of gold and the second bump is formed of solder, a mounting structure of solder bumps with a core (gold) can be easily obtained.

25 (18) According to the present invention, there is provided a circuit board over which the above-described semiconductor device is mounted.

(19) An electronic instrument according to the present invention is provided with the above semiconductor device.

20 (20) According to the present invention, there is provided a method of fabricating a semiconductor device comprising the steps of:

25 preparing a substrate including a plurality of holes and an interconnecting pattern which extends partially over the holes, and also preparing a semiconductor chip having a plurality of electrodes which have conductive members formed on the electrodes; and

disposing the conductive members within the holes and mounting the semiconductor chip over the substrate to connect electrically the interconnecting pattern to the electrodes through the conductive members.

5 According to the present invention, the conductive members formed on the electrodes of the semiconductor chip are disposed within the holes and connected to the interconnecting pattern. Therefore, the interconnecting pattern is located on the side of the substrate opposite to the mounting region of the semiconductor chip. Specifically, since the interconnecting pattern is not covered with the semiconductor chip, the interconnecting pattern can be designed without limitation. Moreover, there is a substrate between the interconnecting pattern and the semiconductor chip. Therefore, signals in an integrated circuit in the semiconductor chip scarcely interfere with signals in the interconnecting pattern, whereby cross talk can be reduced. Because of this, a semiconductor device with an increased degree of freedom in designing the interconnecting pattern can be obtained without 20 decreasing connection reliability.

(21) This method of fabricating a semiconductor device may further comprise a step of providing a resin over the substrate in a region for mounting the semiconductor chip.

According to this semiconductor device, the 25 semiconductor chip is mounted on a surface of the substrate on which the interconnecting pattern is not required, and a resin is provided between the substrate and the semiconductor chip.

Therefore, if an interconnecting pattern is not formed over the surface of the substrate over which the semiconductor chip is mounted, the resin is provided on the substrate exhibiting comparatively excellent adhesion, so that interface 5 delamination can be reduced by the heat in the mounting process. Because of this, a semiconductor device with an increased degree of freedom in designing the interconnecting pattern can be obtained more effectively without decreasing connection reliability.

10 (22) In this method of fabricating a semiconductor device,

the resin may be an anisotropic conductive material containing conductive particles; and

15 after the provision of the resin, the conductive members may be electrically connected to the interconnecting pattern through the conductive particles.

This enables the electrodes of the semiconductor chip to be electrically connected to the interconnecting pattern through the anisotropic conductive material, and, at the same 20 time, the semiconductor chip and the substrate can be underfilled. Therefore, a semiconductor device can be fabricated using a method excelling in productivity.

(23) In this method of fabricating a semiconductor device,

25 the holes may be formed in the substrate to be positioned under the electrodes;

part of the interconnecting pattern may close the holes;

and

the conductive members may be disposed within the holes.

(24) In this method of fabricating a semiconductor device,

5 the interconnecting pattern may include a plurality of interconnecting lines;

two or more of the interconnecting lines may extend over each of the holes in the substrate; and

two or more of the conductive members may be disposed within each of the holes.

This enables to easily form holes necessary for the substrate.

(25) In this method of fabricating a semiconductor device,

the step of providing a resin may include a step of mounting the substrate over a member;

the member may have properties which repel the resin at least in a region facing the holes in the substrate; and

20 the resin may be provided after the mounting of the substrate over the member with a surface of the substrate having the interconnecting pattern to face the member.

This enables the resin to be provided on the substrate without leaking out from slits.

(26) This method of fabricating a semiconductor device
25 may further comprise a step of roughing the other surface of the substrate.

According to this method, since a contact area between

the substrate and the resin increases, adhesion between the resin and the substrate can be further improved.

(27) This method of fabricating a semiconductor device may further comprise a step of forming a recognition hole in 5 the substrate at a position differing from the holes, and forming a recognition pattern over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

This enables the semiconductor chip to be easily mounted over the substrate.

(28) In this method of fabricating a semiconductor device,

the recognition pattern may include a first pattern extending in the X-axis direction of the two-dimensional coordinate system established on a surface of the substrate, and a second pattern extending in the Y-axis direction; and

positioning of the semiconductor chip and the substrate may be carried out by using the recognition pattern.

This enables the semiconductor chip to be accurately 20 mounted at a given position over the substrate by recognizing the first and second patterns.

(29) In this method of fabricating a semiconductor device,

the conductive members may be a plurality of layered 25 bumps.

This enables the conductive members to be reliably formed.

(30) In this method of fabricating a semiconductor device, the bumps may be formed by:

a first step of bonding a first conductive wire to one of the electrodes of the semiconductor chip and cutting the bonded first conductive wire with part of the first conductive wire to remain on the one of the electrodes;

5 a second step of forming a first bump by pressing the remaining part of the first conductive wire on the electrode;

a third step of bonding a second conductive wire to the first bump and cutting the bonded second conductive wire with part of the second conductive wire to remain on the first bump; and

a fourth step of forming a second bump by pressing the remaining part of the second conductive wire on the first bump.

According to this method, the first and second bumps can be layered merely by bonding the first or second conductive wire on the electrode or first bump, cutting the conductive wire while allowing part of the conductive wire to remain on the electrode or first bump, and pressing the remaining conductive wire. 20 These steps can be performed in a short period of time in comparison with the case of layering the bumps by plating.

Note that the first and second bumps refer to two arbitrary bumps, and this is applicable to two or more bumps.

(31) In this method of fabricating a semiconductor 25 device,

the first step may be repeated for the plurality of electrodes to provide each of the electrodes with part of the

first conductive wire; and

the remaining parts of the first conductive wires on the electrodes may be simultaneously pressed to form the first bumps at a time in the second step.

5 According to this method, since a plurality of first bumps can be formed at the same time, the number of steps can be further reduced.

(32) In this method of fabricating a semiconductor device,

10 the third step may be repeated to provide each of the first bumps with part of the second conductive wire; and

the remaining parts of the second conductive wires on the electrodes may be simultaneously pressed to form the second bumps at a time in the fourth step.

15 According to this method, since a plurality of second bumps can be formed at the same time, the number of steps can be further reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

20 Figures 1A to 1C illustrate a method of fabricating a semiconductor device according to a first embodiment of the present invention.

25 Figures 2A and 2B illustrate the method of fabricating a semiconductor device according to the first embodiment of the present invention.

Figures 3A to 3C illustrate the method of fabricating a semiconductor device according to the first embodiment of the

present invention.

Figures 4A and 4B illustrate the method of fabricating a semiconductor device according to the first embodiment of the present invention.

5 Figure 5 shows a semiconductor device according to the first embodiment of the present invention.

Figure 6 shows a substrate according to the first embodiment of the present invention.

10 Figure 7 shows a substrate according to a second embodiment of the present invention.

Figures 8 illustrate a method of fabricating a semiconductor device according to the second embodiment of the present invention.

15 Figures 9A to 9D illustrate a method of fabricating a semiconductor device according to a third embodiment of the present invention.

Figure 10 shows a circuit board on which the semiconductor device according to the present invention is mounted.

20 Figure 11 shows an electronic instrument having the semiconductor device according to the present invention.

Figure 12 shows an electronic instrument having the semiconductor device according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

25 Embodiments of the present invention are described below with reference to the drawings. As the package type of a semiconductor device according to the present invention, any

of BGA (Ball Grid Array), CSP (Chip Size/Scale Package), and the like may be applied. The present invention may be applied to face-down type semiconductor devices and a module structure thereof. As examples of the face-down type semiconductor devices, a COF (Chip On Flex/Film) structure, COB (Chip On Board) structure, and the like can be given. These semiconductor devices not only include semiconductor chips mounted therein, but also may have a module structure in which passive devices such as an SMD (Surface Mount Device) such as a resistance and a capacitor are appropriately included in combination, as described later.

First embodiment

Figures 1A to 4B are views showing a method of fabricating a semiconductor device according to a first embodiment to which the present invention is applied. Figures 1A to 4B show an example of a method of forming bumps on the semiconductor chip. In the present embodiment, bumps are formed on the semiconductor chip as an example of conductive members. Specifically, a plurality of bumps (first and second bumps 70 and 80) is formed on a semiconductor chip 10.

Figures 1A to 2B are views showing a method of forming the first bumps 70. The semiconductor chip 10 with at least one electrode (or pad) 12 formed thereon is prepared, as shown in Figure 1A. Each electrode 12 is generally thin and flat, formed on the first semiconductor chip 10 using aluminum, for example. There are no specific limitations to the shape of the

side surface or vertical cross section of the electrodes 12. The electrodes 12 may be formed at the same height as the semiconductor chip 10. The planar shape of the electrodes 12 is not particularly limited. The electrodes 12 may be either 5 circular or rectangular. A passivation film (not shown) is formed on the semiconductor chip 10 so as to avoid the electrodes 12. The passivation film may be formed using SiO_2 , SiN , polyimide resin, or the like.

A capillary 14 is disposed on the side of a surface of the semiconductor chip 10 on which the electrodes 12 are formed. A conductive wire 16 such as a wire is inserted into the capillary 14. The conductive wire 16 is generally formed using gold, gold-tin, solder, copper, aluminum, or the like, although the material is not limited insofar as the material exhibits conductivity. A ball 17 is formed on the conductive wire 16 outside the capillary 14. The ball 17 is formed by discharging electricity at a high voltage to the end of the conductive wire 16 using an electric flame off, for example.

In the present invention, the conductive wire 16 for 20 forming the first bumps may be called a first conductive wire and the conductive wire 16 for forming the second bumps may be called a second conductive wire.

The capillary 14 is disposed above one of the electrodes 12, thereby disposing the ball 17 above this electrode 12. The 25 capillary 14 is lowered by opening a clamper 18, whereby the ball 12 is pressed against the electrode 12. Ultrasonic waves, heat, and the like are applied while bonding the ball 17 to the

electrode 12 by pressing the ball 17 at a uniform pressure. The conductive wire 16 is thus bonded to the electrode 12 as shown in Figure 1B.

The conductive wire 16 is held by closing the clamper 18.

- 5 The capillary 14 and the clamper 18 are simultaneously lifted as shown in Figure 1C. The conductive wire 16 is torn off, whereby the portion including the ball 17 remains on the electrode 12. In the case where the bumps must be formed on a plurality of electrodes 12, these steps may be repeated for each electrode 12.

Part of the conductive wire 16 remaining on the electrode 12 (including the ball 17) is often has a projected shape due to looping by tearing off the conductive wire 16 on the bonded ball 17.

- The steps shown in Figures 2A and 2B are then carried out. The semiconductor chip 10 on which part of the conductive wire 16 bonded to the electrode 12 (including the ball 17) remains is placed on a stand 20, as shown in Figure 2A. Part of the conductive wire 16 is crushed using a press jig 22, as shown in Figure 2B. In the present embodiment, part of the conductive wires 16 remaining on a plurality of electrodes 12 is crushed at the same time. Note that part of the conductive wire 16 (including the ball 17) may be crushed for each electrode 12 (flattening step). In this step, a bonder for gang bonding or 25 a bonder for single point bonding may be used.

The first bump 70 is thus formed on each electrode 12 as shown in Figure 2B. It is preferable that the upper end of the

first bump 70 be flat by being crushed by the press jig 22. Specifically, the first bump 70 is formed so as to be provided with stability to such an extent that the second bump 80 can be formed on the first bump 70 as described later. A depression section may be formed on the side surface of the first bump 70. The first bump 70 can be prevented from falling off by allowing the depression section to be filled with a resin (see Figure 5) (mechanical anchoring effect). This is also applicable to the second bump 80. In the case of bumps formed on top (third bumps in Figure 5), the flattening step ensures that the upper end of the bumps becomes flat to such an extent that these bumps are securely connected to the interconnecting pattern 32. The flattening step is a measure for enabling the second bumps 80 to be easily formed as described below. In the case where the second bumps 80 can be formed without any problem, the flattening step may be omitted or replaced by a wet back process using heat for melting.

Figures 3A to 4B are views showing a method of forming the second bumps 80. The method of forming the second bumps 80 is the same as the method illustrated in Figures 1A to 2B except that the first bumps 70 are formed on the electrodes 12. In Figure 4B, the second bump 80 is preferably layered on the first bump 70 perpendicularly thereto. It is preferable to reduce unevenness of the bump height by performing the flattening step after forming the second bumps 80. This decreases the failure rate in the step of mounting the semiconductor chip described later.

Note that the first and second bumps 70 and 80 refer to two arbitrary bumps. The present invention is not limited to only two bumps but is applicable to two or more bumps. The semiconductor device according to the present invention has 5 conductive members between the electrodes 12 and the interconnecting pattern 32. The conductive members are not limited to bumps. Figure 5 illustrates the case of using bumps as the conductive members. The first to third bumps 70, 80, and 90 are an arbitrary number of bumps. The number of bumps 10 is not limited. Only one bump may be used as the conductive member. Bumps other than the first bumps 70 such as the second bumps 80 may be formed using a material differing from that for the first bumps 70 according to the method of mounting the semiconductor chip as described later. In the case of forming the first bumps 70 using gold and forming the second bumps 80 using a metal having a melting point lower than gold such as gold-tin or solder, for example, the flattening step after forming the second bumps 80 can be performed using a wet back process by heating for melting or the like, whereby the 15 fabrication steps can be simplified. Note that the semiconductor chips can be mounted using the bumps as a brazing material. Since the existing wire bonders can be utilized in the above ball bump method, the semiconductor device can be fabricated with reduced equipment investment.

20 25 The above step illustrate an example of ball bumps using bonding wire. As a method of forming the bumps, a conventional electroplating technique, electroless plating technique,

paste printing technique, ball placement technique, a combination of these techniques may be used. In the case where two or more bumps are layered, the manufacturing method therefor and a combination of the materials are not limited.

5 Figure 5 is a view showing a semiconductor device according to the present embodiment. Figure 6 is a plan view showing a substrate 30 according to the present embodiment before the semiconductor chip 10 is mounted. A semiconductor device 1 includes the semiconductor chip 10 and the substrate 30.

10 The semiconductor device includes the first and second bumps 70 and 80 formed by the above steps. In the present embodiment, the semiconductor device further includes the third bumps 90. In the present invention, other conductive members may be used in place of bumps.

15 The substrate 30 may be formed using any organic or inorganic material or a composite structure of these materials. The substrate 30 may be used as an individual piece or used in the shape of a strip in which a plurality of mounting regions 20 of the semiconductor chip 10 is formed in a matrix. In the case of using the substrate 30 in the shape of a strip, the substrate 30 is stamped out in another step. As examples of the substrate 30 formed using an organic material, two-layer and three-layer flexible substrates formed of a polyimide resin and the like 25 can be given. A tape used in TAB technology may be used as the flexible substrate. As examples of the substrate 30 formed using an inorganic material, a ceramic substrate, a glass

substrate, and the like can be given. As examples of a substrate formed of a composite structure of organic and inorganic materials, a glass epoxy substrate and the like can be given. There are no specific limitations to the planar shape of the substrate 30. It is preferable that the substrate 30 be similar in shape to the semiconductor chip 10.

30. In the present embodiment, the interconnecting pattern 32 is formed on one surface of the substrate 30. The interconnecting pattern 32 is formed by a plurality of interconnecting lines. Specifically, the interconnecting pattern 32 is formed on the substrate 30 by routing a plurality of interconnecting lines into a specific shape. The interconnecting pattern 32 is generally formed by etching copper foil. The interconnecting pattern 32 may be formed of two or more layers. Copper foil is generally bonded to the substrate 30 in advance through an adhesive (not shown). As another example, the interconnecting pattern 32 may be formed by layering any of copper (Cu), chromium (Cr), titanium (Ti), nickel (Ni), and titanium tungsten (Ti-W). For example, the interconnecting pattern 32 may be formed by etching after applying photolithography. The interconnecting pattern 32 may be directly formed on the substrate 30 by sputtering. In addition, the interconnecting pattern 72 may be formed by plating. Part of the interconnecting pattern 32 may be formed into land sections 37 and 39 having an area larger than the sections which become the lines. The land sections 37 and 39

have a function of sufficiently securing the electrical connections. Therefore, as shown in Figure 6, the land sections 37 may be formed in the connection sections with the electrodes 12, and the land sections 39 may be formed in the connection sections with the external terminals 40 as described later.

A plurality of holes 36 is formed in the substrate 30. The conductive members (first to third bumps 70, 80, and 90) formed on the electrodes 12 of the semiconductor chip 10 are inserted into the holes 36. In this case, the conductive members have a height so as to electrically connect the electrodes 12 of the semiconductor chip 10 to the interconnecting pattern 32 (land sections 37). For example, one bump (first bump 70, for example) may be formed to have a height so as to electrically connect the electrodes 12 to the interconnecting pattern 32. In the case of forming a plurality of bumps, each bump may be formed so that the total height of the layered bumps exceeds the distance between the electrodes 12 and the interconnecting pattern 32.

The holes 36 are formed in the substrate 10 inside the mounting region of the semiconductor chip 10 corresponding to the arrangement and the number of the electrodes 12. For example, the holes 36 may be formed along two sides of the substrate 10 facing each other inside the mounting region of the semiconductor chip 10 corresponding to the electrodes 12 formed along two sides of the semiconductor chip 10 facing each other, as shown in Figure 6. One conductive member may be disposed in one hole 36. The holes 36 have a cross-sectional

area which allows insertion of the conductive members. The shape of the holes 36 may be either circular or rectangular. The holes 36 are formed through the substrate 30. The interconnecting pattern 32 formed on one surface of the substrate 30 close one of the openings of the holes 36. Specifically, the land sections 37 close the opening of the holes 36 on the side of the surface on which the interconnecting pattern 32 is formed. It is preferable that the conductive members be formed to have a height greater than the thickness of the substrate 30 so as to be electrically connected to the interconnecting pattern 32 (land sections 37).

The semiconductor chip 10 is mounted on a surface of the substrate 30 on which the interconnecting pattern 32 is not necessarily required, such that a surface of the semiconductor chip on which the electrodes 12 are formed faces the substrate 30. In the present embodiment, the interconnecting pattern 32 is not formed on the surface of the substrate 30 on which the semiconductor chip 10 is mounted. The conductive members formed on the electrodes 12 are inserted into the holes 36 and electrically connected to the interconnecting pattern 32 (land sections 37) formed on one of the openings of the holes 36. Specifically, the conductive members are electrically connected to the interconnecting pattern 32 (land sections 37) exposed by the holes 36. The semiconductor device according to the present invention has conductive members between the electrodes 12 and the interconnecting pattern 32. The conductive members are not limited to bumps. As examples of

other conductive members, conductive paste, conductive balls, and the like can be given. The conductive members may be formed on the interconnecting pattern 32 (land sections 37) exposed by the holes 36. Both of these conductive members and the 5 conductive members formed on the semiconductor chip 10 may be used as the conductive members.

10
15
20
25

According to this semiconductor device, the conductive members formed on the electrodes 12 of the first semiconductor chip 10 are disposed in the holes 36 and connected to the interconnecting pattern 32. This allows the interconnecting pattern 32 to be located on a surface of the substrate 30 opposite to the mounting region of the semiconductor chip 10. Specifically, since the interconnecting pattern 32 is not covered with the semiconductor chip 10, the interconnecting pattern 32 can be designed without limitation. The interconnecting pattern 32 is formed opposite the semiconductor chip 10 through the substrate 30. Therefore, signals in an integrated circuit in the semiconductor chip 10 scarcely interfere with signals in the interconnecting pattern 32, whereby cross talk can be reduced. Because of this, a 20 semiconductor device with an increased degree of freedom in designing the interconnecting pattern 32 can be obtained without decreasing connection reliability.

A resin is provided between the semiconductor chip 10 and 25 the substrate 30. Specifically, in the present embodiment, a resin is provided to the surface of the substrate 30 on which the interconnecting pattern 32 is not formed and within at least

the mounting region (including holes 36) of the semiconductor chip 10. In the present embodiment, the resin is an anisotropic conductive material 34. The anisotropic conductive material 34 is prepared by dispersing conductive particles (fillers) in an adhesive (binder). A dispersing agent may be added to the anisotropic conductive material 34. A heat-curable adhesive is generally used as the adhesive for the anisotropic conductive material 34. As the anisotropic conductive material 34, an anisotropic conductive film previously formed into a sheet is generally used. In addition, a liquid anisotropic conductive material may be used. The anisotropic conductive material 34 is pressed between the conductive members and the interconnecting pattern 32, thereby establishing electrical connection between them through the conductive particles. The present invention is not limited to this configuration. As the method for establishing electrical connection between the conductive members and the interconnecting pattern 32, a method using a metal junction such as Au-Au, Au-Sn, or solder, a method using conductive resin paste, a method utilizing the shrinkage force of an insulating resin, and the like can be given. Any of these methods may be used.

In the case of employing any mounting method, an insulating resin is generally sealed at least between the substrate 30 and the semiconductor chip 10. According to this semiconductor device, the semiconductor chip 10 is mounted on a surface of the substrate 30 on which the interconnecting pattern 32 is not necessarily required, and the resin is

provided between the substrate 30 and the semiconductor chip 10. Therefore, even if the interconnecting pattern 32 is not formed on a surface of the substrate 30 on which the semiconductor chip 10 is mounted, delamination can be prevented
5 since the resin is provided on the substrate 30 exhibiting comparatively excellent adhesion. The substrate 50 is interposed between the semiconductor chip 10 and the interconnecting pattern 32. Therefore, in the case of forming the substrate 30 using a soft material, the substrate 30 can absorb stress applied to the semiconductor chip 10 and the interconnecting pattern 32. Because of this, a semiconductor device with an increased degree of freedom in designing the interconnecting pattern 32 can be obtained more effectively without decreasing connection reliability.

At least the region of the substrate 30 in which the anisotropic conductive material 34 is provided may be roughed. Specifically, the surface of the substrate 30 may be roughed so as to impair flatness. The surface of the substrate 30 may be roughed mechanically by sandblasting, physically using
20 plasma, ultraviolet rays, or ozone, or chemically using an etching material. This enables the substrate 30 to be bonded to the anisotropic conductive material 34 more securely by increasing the bonding area between the substrate 30 and the anisotropic conductive material 34 or increasing the physical
25 and chemical adhesive force.

A recognition hole 50 and recognition patterns 52 and 54 formed on the recognition hole 50 may be provided to the

substrate 30, as shown in Figure 6. The conductive members can be easily and securely inserted into the holes 36 by using the recognition hole 50 and the recognition patterns 52 and 54. Therefore, it is preferable that the recognition hole 50 and 5 the recognition patterns 52 and 54 be formed in a region of the substrate 30 other than the mounting region of the semiconductor chip 10. The shape and size of the recognition hole 50 are not limited insofar as the recognition patterns 52 and 54 can be recognized. The recognition patterns 52 and 54 may be formed across the recognition hole 50 as shown in Figure 6. The shape of the recognition patterns 52 and 54 is not limited thereto. The recognition patterns 52 and 54 are formed within the recognition hole 50 on a surface of the substrate 30 on which the interconnecting pattern 32 is formed. In the case where the substrate 30 exhibits light transmissibility, the recognition hole 50 is not necessarily formed. In this case, the recognition patterns 52 and 54 are recognized through the substrate 30.

For example, the recognition patterns 52 and 54 may be 20 formed by the first pattern 52 extending in the X-axis direction of the two-dimensional coordinates established on the surface of the substrate 30 and the second pattern 54 extending in the Y-axis direction. The recognition patterns 52 and 54 preferably have a structure so that the position of the 25 semiconductor chip 10 can be recognized two-dimensionally on the surface of the substrate. Part or all of the land sections 39, external terminals 40, and interconnecting pattern 32 may

be used as the recognition patterns 52 and 54. The holes 36 or marks formed by printing, laser processing, or the like may be used as the recognition patterns 52 and 54.

A plurality of external terminals 40 may be formed on a surface of the interconnecting pattern 32 opposite to the surface facing the substrate 30. The external terminals 40 may be formed in the land sections 39 of the interconnecting pattern 32. A protective film 33 may be formed on the surface of the interconnect patter 32 on which the external terminals 40 are formed except the area of the external terminals 40. It is preferable that the protective film 33 be an insulating member such as solder resist. In particular, the protective film 33 covers and protects the surface of the interconnecting pattern 32.

10
15
20
25

The external terminals 40 may be formed using solder, a metal other than solder, a conductive resin, or the like. Figure 5 shows a FAN-IN semiconductor device in which the external terminals 40 are formed only in the mounting region of the semiconductor chip 10. However, the present invention is not limited thereto. For example, the present invention may be applied to a FAN-OUT semiconductor device in which the external terminals 40 are formed only outside the mounting region of the semiconductor chip 10, or to a FAN-IN/OUT semiconductor device including the FAN-OUT semiconductor device and FAN-IN semiconductor device in combination.

The method of fabricating the semiconductor device after the step of forming the bumps on the semiconductor chip 10 is

described below.

The semiconductor chip 10 is mounted on the substrate 30. Specifically, a surface of the semiconductor chip 10 on which the electrodes 12 are formed faces a surface of the substrate 30 opposite to the surface on which the interconnecting pattern 32 is required to be formed. Part of the surface of the substrate 30 may be roughed by sandblasting or plasma.

In the case where the resin is the anisotropic conductive material 34, the anisotropic conductive material 34 is previously provided to the substrate 30 before mounting the semiconductor chip 10. Specifically, the anisotropic conductive material 34 is provided to the substrate 30, thereby allowing the conductive members to be electrically connected to the interconnecting pattern 32. According to the present embodiment, the electrodes 12 are electrically connected to the interconnecting pattern 32 through the anisotropic conductive material 34, and, at the same time, the semiconductor chip 10 and the substrate 30 can be underfilled. Therefore, the semiconductor device can be fabricated using a method excelling in reliability and productivity. In the case where the anisotropic conductive material 34 is heat-curable, the substrate 30 and the semiconductor chip 10 can be bonded by curing the anisotropic conductive material 34 using heat after mounting the semiconductor chip 10.

In the case where the recognition hole 50 and the recognition patterns 52 and 54 are formed on the substrate 30, the semiconductor chip 10 can be positioned on the substrate

30 by recognizing the recognition hole 50 and the recognition patterns 52 and 54. For example, the recognition patterns 52 and 54 are formed by the first pattern 52 extending in the X-axis direction of the two-dimensional coordinates established on the 5 surface of the substrate 30 and the second pattern 54 extending in the Y-axis direction, as shown in Figure 6. In this case, the semiconductor chip 10 can be positioned on the substrate 30 by finding the Y coordinates on the surface of the substrate by recognizing the recognition pattern 52 and finding the X coordinates by recognizing the recognition pattern 54. This enables the semiconductor chip 10 to be accurately mounted at a specific position on the substrate 30.

The step of providing the resin may be performed after mounting the semiconductor chip 10 excluding the case where the anisotropic conductive material 34 is used as the resin. In this case, the semiconductor chip 10 and the substrate 30 may be underfilled by filling the space between the semiconductor chip 10 and the substrate 30 with the resin while removing bubbles, for example.

20 A plurality of external terminals 40 may be formed on the interconnecting pattern 32. Specifically, the external terminals 40 are formed on surface of the interconnecting pattern 32 opposite to the surface facing the substrate. For example, the external terminals 40 are formed in the land 25 sections 39, as shown in Figure 6. The external terminals 40 may be formed using a conductive material such as solder or a metal. In the present embodiment, the external terminals 40

are solder balls. The solder balls are formed by a reflow process consisting of providing solder balls and flux, cream solder, or the like and melting the solder by heating. Therefore, the above heating step for the anisotropic 5 conductive material 34 (in the case of heat-curable material) may be omitted, and formation of the solder balls and heating for the anisotropic conductive material 74 may be performed at the same time in this reflow process. In addition, other passive devices to be mounted on the substrate 30 may be soldered at the same time.

Second embodiment

Figure 7 is a plan view showing the substrate 30 according to the present embodiment before the semiconductor chip 10 is mounted. The present embodiment differs from the first embodiment as to the configuration of the holes. In the present embodiment, the holes are slits 38. Long, narrow slits 38 are formed. Part of the interconnecting pattern 32 is formed across the slits 38 in the direction of the width of the slits 38. 20 Specifically, two or more interconnecting lines among a plurality of interconnecting lines are formed across the slits 38.

The slits 38 are formed corresponding to the rows of each electrode 12 of the semiconductor chip 10. For example, two 25 slits 38 may be formed in the substrate 10 along two sides of the mounting region of the semiconductor chip 10 facing each other corresponding to the electrodes 12 formed along two sides

of the semiconductor chip 10 facing each other, as shown in Figure 7. A plurality of electrodes 12 may be disposed on one slit 38. Specifically, two or more conductive members formed on the electrodes 12 may be inserted into one slit. The size and shape of the slits 38 may be optionally determined according to the arrangement of the electrodes 12. This enables necessary holes to be easily formed in the substrate 30 in comparison with the case of forming holes corresponding to each electrode 12. The slits 38 may be divided as required. Other structures are the same as those in the first embodiment.

A method of fabricating the semiconductor device according to the present embodiment is described below. In the present embodiment, the same steps as in the first embodiment can be performed except for the steps relating to the slits 38 formed in the substrate 30.

Step of providing resin

In this step, a resin is provided to the substrate 30. The resin is provided to the substrate 30 at least in the mounting region of the semiconductor chip 10. The resin (anisotropic conductive material 34, for example) may be provided before mounting the semiconductor chip 10 on the substrate 30. The resin may be provided after mounting the semiconductor chip 10.

In the present embodiment, the slits 38 are formed in the substrate 30. Part of the slits 38 is an opening. Therefore, a member is provided as an underlay to the side of the substrate 30 on which the interconnecting pattern 32 is formed before

providing a resin to the substrate 30. In other words, the opening of the slits 38 is closed by placing the substrate 30 on the member. The member preferably exhibits no affinity (or low affinity) to the resin to such an extent that the resin is
5 not allowed to permeate into the member at least in the region of the substrate 30 in which the slits 38 are disposed. Specifically, the member preferably has properties for repelling the resin. This enables the resin to be provided on the substrate 30 without allowing the resin to leak out or to penetrate into the member. This is particularly effective when preparing the resin as liquid or gel.

100
105
110
115
120
125
130
135
140
145
150
155
160
165
170
175
180
185
190
195
200
205
210
215
220
225
230
235
240
245
250
255
260
265
270
275
280
285
290
295
300
305
310
315
320
325
330
335
340
345
350
355
360
365
370
375
380
385
390
395
400
405
410
415
420
425
430
435
440
445
450
455
460
465
470
475
480
485
490
495
500
505
510
515
520
525
530
535
540
545
550
555
560
565
570
575
580
585
590
595
600
605
610
615
620
625
630
635
640
645
650
655
660
665
670
675
680
685
690
695
700
705
710
715
720
725
730
735
740
745
750
755
760
765
770
775
780
785
790
795
800
805
810
815
820
825
830
835
840
845
850
855
860
865
870
875
880
885
890
895
900
905
910
915
920
925
930
935
940
945
950
955
960
965
970
975
980
985
990
995
1000
1005
1010
1015
1020
1025
1030
1035
1040
1045
1050
1055
1060
1065
1070
1075
1080
1085
1090
1095
1100
1105
1110
1115
1120
1125
1130
1135
1140
1145
1150
1155
1160
1165
1170
1175
1180
1185
1190
1195
1200
1205
1210
1215
1220
1225
1230
1235
1240
1245
1250
1255
1260
1265
1270
1275
1280
1285
1290
1295
1300
1305
1310
1315
1320
1325
1330
1335
1340
1345
1350
1355
1360
1365
1370
1375
1380
1385
1390
1395
1400
1405
1410
1415
1420
1425
1430
1435
1440
1445
1450
1455
1460
1465
1470
1475
1480
1485
1490
1495
1500
1505
1510
1515
1520
1525
1530
1535
1540
1545
1550
1555
1560
1565
1570
1575
1580
1585
1590
1595
1600
1605
1610
1615
1620
1625
1630
1635
1640
1645
1650
1655
1660
1665
1670
1675
1680
1685
1690
1695
1700
1705
1710
1715
1720
1725
1730
1735
1740
1745
1750
1755
1760
1765
1770
1775
1780
1785
1790
1795
1800
1805
1810
1815
1820
1825
1830
1835
1840
1845
1850
1855
1860
1865
1870
1875
1880
1885
1890
1895
1900
1905
1910
1915
1920
1925
1930
1935
1940
1945
1950
1955
1960
1965
1970
1975
1980
1985
1990
1995
2000
2005
2010
2015
2020
2025
2030
2035
2040
2045
2050
2055
2060
2065
2070
2075
2080
2085
2090
2095
2100
2105
2110
2115
2120
2125
2130
2135
2140
2145
2150
2155
2160
2165
2170
2175
2180
2185
2190
2195
2200
2205
2210
2215
2220
2225
2230
2235
2240
2245
2250
2255
2260
2265
2270
2275
2280
2285
2290
2295
2300
2305
2310
2315
2320
2325
2330
2335
2340
2345
2350
2355
2360
2365
2370
2375
2380
2385
2390
2395
2400
2405
2410
2415
2420
2425
2430
2435
2440
2445
2450
2455
2460
2465
2470
2475
2480
2485
2490
2495
2500
2505
2510
2515
2520
2525
2530
2535
2540
2545
2550
2555
2560
2565
2570
2575
2580
2585
2590
2595
2600
2605
2610
2615
2620
2625
2630
2635
2640
2645
2650
2655
2660
2665
2670
2675
2680
2685
2690
2695
2700
2705
2710
2715
2720
2725
2730
2735
2740
2745
2750
2755
2760
2765
2770
2775
2780
2785
2790
2795
2800
2805
2810
2815
2820
2825
2830
2835
2840
2845
2850
2855
2860
2865
2870
2875
2880
2885
2890
2895
2900
2905
2910
2915
2920
2925
2930
2935
2940
2945
2950
2955
2960
2965
2970
2975
2980
2985
2990
2995
3000
3005
3010
3015
3020
3025
3030
3035
3040
3045
3050
3055
3060
3065
3070
3075
3080
3085
3090
3095
3100
3105
3110
3115
3120
3125
3130
3135
3140
3145
3150
3155
3160
3165
3170
3175
3180
3185
3190
3195
3200
3205
3210
3215
3220
3225
3230
3235
3240
3245
3250
3255
3260
3265
3270
3275
3280
3285
3290
3295
3300
3305
3310
3315
3320
3325
3330
3335
3340
3345
3350
3355
3360
3365
3370
3375
3380
3385
3390
3395
3400
3405
3410
3415
3420
3425
3430
3435
3440
3445
3450
3455
3460
3465
3470
3475
3480
3485
3490
3495
3500
3505
3510
3515
3520
3525
3530
3535
3540
3545
3550
3555
3560
3565
3570
3575
3580
3585
3590
3595
3600
3605
3610
3615
3620
3625
3630
3635
3640
3645
3650
3655
3660
3665
3670
3675
3680
3685
3690
3695
3700
3705
3710
3715
3720
3725
3730
3735
3740
3745
3750
3755
3760
3765
3770
3775
3780
3785
3790
3795
3800
3805
3810
3815
3820
3825
3830
3835
3840
3845
3850
3855
3860
3865
3870
3875
3880
3885
3890
3895
3900
3905
3910
3915
3920
3925
3930
3935
3940
3945
3950
3955
3960
3965
3970
3975
3980
3985
3990
3995
4000
4005
4010
4015
4020
4025
4030
4035
4040
4045
4050
4055
4060
4065
4070
4075
4080
4085
4090
4095
4100
4105
4110
4115
4120
4125
4130
4135
4140
4145
4150
4155
4160
4165
4170
4175
4180
4185
4190
4195
4200
4205
4210
4215
4220
4225
4230
4235
4240
4245
4250
4255
4260
4265
4270
4275
4280
4285
4290
4295
4300
4305
4310
4315
4320
4325
4330
4335
4340
4345
4350
4355
4360
4365
4370
4375
4380
4385
4390
4395
4400
4405
4410
4415
4420
4425
4430
4435
4440
4445
4450
4455
4460
4465
4470
4475
4480
4485
4490
4495
4500
4505
4510
4515
4520
4525
4530
4535
4540
4545
4550
4555
4560
4565
4570
4575
4580
4585
4590
4595
4600
4605
4610
4615
4620
4625
4630
4635
4640
4645
4650
4655
4660
4665
4670
4675
4680
4685
4690
4695
4700
4705
4710
4715
4720
4725
4730
4735
4740
4745
4750
4755
4760
4765
4770
4775
4780
4785
4790
4795
4800
4805
4810
4815
4820
4825
4830
4835
4840
4845
4850
4855
4860
4865
4870
4875
4880
4885
4890
4895
4900
4905
4910
4915
4920
4925
4930
4935
4940
4945
4950
4955
4960
4965
4970
4975
4980
4985
4990
4995
5000
5005
5010
5015
5020
5025
5030
5035
5040
5045
5050
5055
5060
5065
5070
5075
5080
5085
5090
5095
5100
5105
5110
5115
5120
5125
5130
5135
5140
5145
5150
5155
5160
5165
5170
5175
5180
5185
5190
5195
5200
5205
5210
5215
5220
5225
5230
5235
5240
5245
5250
5255
5260
5265
5270
5275
5280
5285
5290
5295
5300
5305
5310
5315
5320
5325
5330
5335
5340
5345
5350
5355
5360
5365
5370
5375
5380
5385
5390
5395
5400
5405
5410
5415
5420
5425
5430
5435
5440
5445
5450
5455
5460
5465
5470
5475
5480
5485
5490
5495
5500
5505
5510
5515
5520
5525
5530
5535
5540
5545
5550
5555
5560
5565
5570
5575
5580
5585
5590
5595
5600
5605
5610
5615
5620
5625
5630
5635
5640
5645
5650
5655
5660
5665
5670
5675
5680
5685
5690
5695
5700
5705
5710
5715
5720
5725
5730
5735
5740
5745
5750
5755
5760
5765
5770
5775
5780
5785
5790
5795
5800
5805
5810
5815
5820
5825
5830
5835
5840
5845
5850
5855
5860
5865
5870
5875
5880
5885
5890
5895
5900
5905
5910
5915
5920
5925
5930
5935
5940
5945
5950
5955
5960
5965
5970
5975
5980
5985
5990
5995
6000
6005
6010
6015
6020
6025
6030
6035
6040
6045
6050
6055
6060
6065
6070
6075
6080
6085
6090
6095
6100
6105
6110
6115
6120
6125
6130
6135
6140
6145
6150
6155
6160
6165
6170
6175
6180
6185
6190
6195
6200
6205
6210
6215
6220
6225
6230
6235
6240
6245
6250
6255
6260
6265
6270
6275
6280
6285
6290
6295
6300
6305
6310
6315
6320
6325
6330
6335
6340
6345
6350
6355
6360
6365
6370
6375
6380
6385
6390
6395
6400
6405
6410
6415
6420
6425
6430
6435
6440
6445
6450
6455
6460
6465
6470
6475
6480
6485
6490
6495
6500
6505
6510
6515
6520
6525
6530
6535
6540
6545
6550
6555
6560
6565
6570
6575
6580
6585
6590
6595
6600
6605
6610
6615
6620
6625
6630
6635
6640
6645
6650
6655
6660
6665
6670
6675
6680
6685
6690
6695
6700
6705
6710
6715
6720
6725
6730
6735
6740
6745
6750
6755
6760
6765
6770
6775
6780
6785
6790
6795
6800
6805
6810
6815
6820
6825
6830
6835
6840
6845
6850
6855
6860
6865
6870
6875
6880
6885
6890
6895
6900
6905
6910
6915
6920
6925
6930
6935
6940
6945
6950
6955
6960
6965
6970
6975
6980
6985
6990
6995
7000
7005
7010
7015
7020
7025
7030
7035
7040
7045
7050
7055
7060
7065
7070
7075
7080
7085
7090
7095
7100
7105
7110
7115
7120
7125
7130
7135
7140
7145
7150
7155
7160
7165
7170
7175
7180
7185
7190
7195
7200
7205
7210
7215
7220
7225
7230
7235
7240
7245
7250
7255
7260
7265
7270
7275
7280
7285
7290
7295
7300
7305
7310
7315
7320
7325
7330
7335
7340
7345
7350
7355
7360
7365
7370
7375
7380
7385
7390
7395
7400
7405
7410
7415
7420
7425
7430
7435
7440
7445
7450
7455
7460
7465
7470
7475
7480
7485
7490
7495
7500
7505
7510
7515
7520
7525
7530
7535
7540
7545
7550
7555
7560
7565
7570
7575
7580
7585
7590
7595
7600
7605
7610
7615
7620
7625
7630
7635
7640
7645
7650
7655
7660
7665
7670
7675
7680
7685
7690
7695
7700
7705
7710
7715
7720
7725
7730
7735
7740
7745
7750
7755
7760
7765
7770
7775
7780
7785
7790
7795
7800
7805
7810
7815
7820
7825
7830
7835
7840
7845
7850
7855
7860
7865
7870
7875
7880
7885
7890
7895
7900
7905
7910
7915
7920
7925
7930
7935
7940
7945
7950
7955
7960
7965
7970
7975
7980
7985
7990
7995
8000
8005
8010
8015
8020
8025
8030
8035
8040
8045
8050
8055
8060
8065
8070
8075
8080
8085
8090
8095
8100
8105
8110
8115
8120
8125
8130
8135
8140
8145
8150
8155
8160
8165
8170
8175
8180
8185
8190
8195
8200
8205
8210
8215
8220
8225
8230
8235
8240
8245
8250
8255
8260
8265
8270
8275
8280
8285
8290
8295
8300
8305
8310
8315
8320
8325
8330
8335
8340
8345
8350
8355
8360
8365
8370
8375
8380
8385
8390
8395
8400
8405
8410
8415
8420
8425
8430
8435
8440
8445
8450
8455
8460
8465
8470
8475
8480
8485
8490
8495
8500
8505
8510
8515
8520
8525
8530
8535
8540
8545
8550
8555
8560
8565
8570
8575
8580
8585
8590
8595
8600
8605
8610
8615
8620
8625
8630
8635
8640
8645
8650
8655
8660
8665
8670
8675
8680
8685
8690
8695
8700
8705
8710
8715
8720
8725
8730
8735
8740
8745
8750
8755
8760
8765
8770
8775
8780
8785
8790
8795
8800
8805
8810
8815
8820
8825
8830
8835
8840
8845
8850
8855
8860
8865
8870
8875
8880
8885
8890
8895
8900
8905
8910
8915
8920
8925
8930
8935
8940
8945
8950
8955
8960
8965
8970
8975
8980
8985
8990
8995
9000
9005
9010
9015
9020
9025
9030
9035
9040
9045
9050
9055
9060
9065
9070
9075
9080
9085
9090
9095
9100
9105
9110
9115
9120
9125
9130
9135
9140
9145
9150
9155
9160
9165
9170
9175
9180
9185
9190
9195
9200
9205
9210
9215
9220
9225
9230
9235
9240
9245
9250
9255
9260
9265
9270
9275
9280
9285
9290
9295
9300
9305
9310
9315
9320
9325
9330
9335
9340
9345
9350
9355
9360
9365
9370
9375
9380
9385
9390
9395
9400
9405
9410
9415
9420
9425
9430
9435
9440
9445
9450
9455
9460
9465
9470
9475
9480
9485
9490
9495
9500
9505
9510
9515
9520
9525
9530
9535
9540
9545
9550
9555
9560
9565
957

is formed opposite the semiconductor chip 10 through the substrate 30. Therefore, signals in the integrated circuit in the semiconductor chip 10 scarcely interfere with signals in the interconnecting pattern 32, whereby cross talk can be
5 reduced. Because of this, a semiconductor device with an increased degree of freedom in designing the interconnecting pattern 32 can be obtained without decreasing connection reliability.

10 **Third embodiment**

Figures 9A to 9D are views showing a method of fabricating a semiconductor device according to the present embodiment. In the present embodiment, a semiconductor device shown in Figure 9D includes the semiconductor chip 10, substrate 30, and external terminals 40.

The substrate 30 is the same as described above. The substrate 30 may be any of a substrate formed using an organic material such as a flexible substrate, a substrate formed using an inorganic material such as a metal substrate, and a
20 combination of these. Through-holes 31 are formed in the substrate 30. The interconnecting pattern 32 is formed to extend over the through-holes 31. Land sections for forming the external terminals (not shown) may be formed on the through-holes 31 as part of the interconnecting pattern 32.

25 After preparing the substrate 30 in this manner, the anisotropic conductive material 34 is provided to the substrate 30. The anisotropic conductive material 34 may be provided in

the area greater than the area of the electrodes 12 in the semiconductor chip 10.

The semiconductor chip 10 is placed on the anisotropic conductive material 34. Specifically, the semiconductor chip 10 is placed on the anisotropic conductive material 34 with the surface on which the electrodes 12 are formed facing the anisotropic conductive material 34. In the present embodiment, the first and second bumps 70 and 80 are formed on the electrode 12. The method for forming these bumps is the same as described above. The second bumps 80 may be formed using a material differing from that for the first bumps 70. For example, the first bumps 70 may be formed using gold, and the second bumps 80 may be formed using gold-tin or a metal having a melting point lower than gold such as solder. Advantage thereof is the same as described above. The semiconductor chip 10 is disposed so that the electrodes 12 are located on the land sections for connecting terminals (not shown) of the interconnecting pattern 32. The first and second bumps 70 and 80 may be formed on the side of the interconnecting pattern 32.

As a result of these steps, the anisotropic conductive material 34 is interposed between the surface of the semiconductor chip 10 on which the electrodes 12 are formed and the surface of the substrate 30 on which the interconnecting pattern 32 is formed. The semiconductor chip 10 is pressed against the substrate 30 by pressing the surface of the semiconductor chip 10 opposite to the surface on which the electrodes 12 are formed using the jig 110. The jig 110 may

have a heating means such as a heater. The semiconductor chips 10 may be heated using the heating means. It is preferable to use a jig having a planar area greater than that of the semiconductor chip 10 as the jig 110 in order to also apply heat 5 to the anisotropic conductive material 34 located outside the semiconductor chip 10. This enables heat to be easily applied to the periphery of the semiconductor chip 10.

Since the semiconductor chip 10 is heated by the jig 110, the adhesive in the anisotropic conductive material 34 is cured in the region in contact with the semiconductor chip 10. Note that the adhesive in the anisotropic conductive material 34 is not completely cured in the region not in contact with the semiconductor chip 10 or in the region apart from the semiconductor chip 10 since heat does not reach. The adhesive in these regions are cured in the next step.

In the case of forming the external terminals 40 using solder, for example, solder 42 is provided in the through-holes 31 in the substrate 30 and the vicinity thereof. The solder 42 may be provided by a printing method using cream solder, for 20 example. Solder balls formed in advance may be placed on the above position.

The solder 34 is heated in a reflow process, thereby forming the external terminals 40, as shown in Figure 9D. In this reflow process, not only the solder 42 but also the 25 anisotropic conductive material 34 are heated. Uncured regions of the anisotropic conductive material 34 are cured by this heating. Specifically, the anisotropic conductive

material 34 is cured in the region not in contact with the semiconductor chip 10 or in the region apart from the semiconductor chip 10 in the reflow process for forming the external terminals 40.

5 According to the semiconductor device thus obtained, since the interval between the semiconductor chip 10 and the substrate 30 is increased by the height of the first and second bumps 70 and 80 formed on the electrodes 12 of the semiconductor chip 10, a large amount of resin can be provided right under the semiconductor chips 10. This allows the resin to fully function as a stress relaxation layer. In the present embodiment, the first and second bumps 70 and 80 refer to an arbitrary number of bumps. The present embodiment is applicable to at least two bumps. In the present invention, the electrical connections between the electrodes 12 and the interconnecting pattern 32 are not limited to the anisotropic conductive material 34, to which various configurations (described above) may be applied.

10 In all of the above embodiments, a semiconductor device having external terminals is described. Part of the substrate may be extended and the external connection may be established therefrom. Part of the substrate 30 may be used as leads for connectors, or connectors may be mounted on the substrate 30. In addition, the interconnecting pattern 32 of the substrate 25 30 may be connected to other electronic instruments.

Instead of positively forming the external terminals 40, the external terminals may be formed using solder cream applied

to a motherboard when mounting the semiconductor device on the motherboard due to surface tension during melting. Such a semiconductor device is referred to as a land grid array semiconductor device. In all of the above embodiments, a 5 plurality of semiconductor chips may be mounted, or semiconductor chips and passive devices may be mounted in combination.

Figure 8 is a view showing a circuit board 1000 provided with the semiconductor device 1 according to the present embodiment. An organic substrate such as a glass epoxy substrate is generally used as the circuit board 1000. Interconnecting pattern is formed on the circuit board 1000 using copper, for example, so as to form a desired circuit. Electrical continuity between the interconnecting pattern and the semiconductor device 1 is established by mechanically connecting the interconnecting pattern to the external terminals 40 of the semiconductor device 1.

Figures 10 and 11 respectively show a notebook-type personal computer and a portable telephone as examples of the 20 electronic instrument provided with the semiconductor device 1 to which the present invention is applied.

In the above embodiments, a semiconductor chip and a semiconductor device using the semiconductor chip are described. The present invention is applicable to all embodiments of an 25 electronic chip using projections.

Note that the "semiconductor chip" that is a structural component of the present invention could be replaced by an

"electronic element," and electronic elements (either active elements or passive elements) can be mounted on a substrate to fabricate an electronic component, in a manner similar to that of semiconductor chips. Examples of electronic components 5 fabricated by using such electronic elements include optical elements, resistors, capacitors, coils, oscillators, filters, temperature sensors, thermistors, varistors, variable resistors, or fuses, by way of example.

All of the above-described embodiments may be applied to a semiconductor device (or mounted module) in which semiconductor chips and other electronic elements as described above are mounted on a substrate in combination.

CLAIMS

1. A semiconductor device comprising:
a substrate including a plurality of holes and a surface
5 over which an interconnecting pattern is formed, part of the
interconnecting pattern being superposed over the holes;
a semiconductor chip disposed over another surface of the
substrate and including a plurality of electrodes to be
positioned over the holes; and
10 conductive members provided within the holes for
electrically connecting the electrodes to the interconnecting
pattern.
2. The semiconductor device as defined in claim 1,
wherein a resin is provided between the substrate and the
semiconductor chip.
3. The semiconductor device as defined in claim 2,
wherein the resin is an anisotropic conductive material
20 containing conductive particles; and
wherein the conductive members are electrically
connected to the interconnecting pattern through the conductive
particles.
- 25 4. The semiconductor device as defined in claim 1,
wherein part of the interconnecting pattern closes the
holes.

5. The semiconductor device as defined in claim 1,
wherein the interconnecting pattern includes a plurality
of interconnecting lines; and
5 wherein two or more interconnecting lines extend over
each of the holes.

6. The semiconductor device as defined in claim 1,
wherein the other surface of the substrate is roughed.

10 7. The semiconductor device as defined in any one of claims
1 to 6,

wherein a recognition hole is formed in the substrate at
a position differing from the holes; and
15 wherein a recognition pattern is formed over the
recognition hole on the side of a surface of the substrate
including the interconnecting pattern.

20 8. The semiconductor device as defined in claim 7,
wherein the recognition hole is formed in the substrate
outside a mounting region for the semiconductor chip.

25 9. The semiconductor device as defined in claim 7,
wherein the recognition pattern includes:
a first pattern extending in the X-axis direction of the
two-dimensional coordinate system established on a surface of
the substrate; and

a second pattern extending in the Y-axis direction.

10. The semiconductor device as defined in any one of claims
1 to 6,

5 wherein the conductive members are a plurality of layered
bumps.

11. The semiconductor device as defined in claim 10,
wherein the bumps include first bumps formed on the
10 electrodes and second bumps formed on the first bumps.

12. The semiconductor device as defined in claim 11,
wherein at least the first bumps are ball bumps.

15 13. The semiconductor device as defined in claim 11,
wherein the second bumps are formed of a metal which has
a melting point lower than the melting point of the first bumps.

14. The semiconductor device as defined in claim 13,
20 wherein the first bumps are formed of gold.

15. The semiconductor device as defined in claim 14,
wherein the second bumps are formed of solder.

25 16. The semiconductor device as defined in claim 11,
wherein the first bumps and the second bumps are formed
of the same material.

17. The semiconductor device as defined in any one of claims
1 to 6,

5 wherein the semiconductor chip is mounted face-down to
the substrate.

18. A circuit board over which is mounted the semiconductor
device as defined in any one of claims 1 to 6.

10 19. An electronic instrument provided with the semiconductor
device as defined in any one of claims 1 to 6.

15 20. A method of fabricating a semiconductor device comprising
the steps of:

preparing a substrate including a plurality of holes and
an interconnecting pattern which extends partially over the
holes, and also preparing a semiconductor chip having a
plurality of electrodes which have conductive members formed
on the electrodes; and

20 disposing the conductive members within the holes and
mounting the semiconductor chip over the substrate to connect
electrically the interconnecting pattern to the electrodes
through the conductive members.

25 21. The method of fabricating a semiconductor device as
defined in claim 20, further comprising
a step of providing a resin over the substrate in a region

for mounting the semiconductor chip.

22. The method of fabricating a semiconductor device as defined in claim 21,

5 wherein the resin is an anisotropic conductive material containing conductive particles; and

wherein after the provision of the resin, the conductive members are electrically connected to the interconnecting pattern through the conductive particles.

10 23. The method of fabricating a semiconductor device as defined in claim 20,

wherein the holes are formed in the substrate to be positioned under the electrodes;

15 wherein part of the interconnecting pattern closes the holes; and

wherein the conductive members is disposed within the holes.

20 24. The method of fabricating a semiconductor device as defined in claim 21,

wherein the interconnecting pattern includes a plurality of interconnecting lines;

25 wherein two or more of the interconnecting lines extend over each of the holes in the substrate; and

wherein two or more of the conductive members are disposed within each of the holes.

25. The method of fabricating a semiconductor device as defined in claim 24,

5 wherein the step of providing a resin includes a step of mounting the substrate over a member;

 wherein the member has properties which repel the resin at least in a region facing the holes in the substrate; and

 wherein the resin is provided after the mounting of the substrate over the member with a surface of the substrate having the interconnecting pattern to face the member.

10 26. The method of fabricating a semiconductor device as defined in claim 20, further comprising

 a step of roughing the other surface of the substrate.

15 27. The method of fabricating a semiconductor device as defined in any one of claims 20 to 26, further comprising

 a step of forming a recognition hole in the substrate at a position differing from the holes, and forming a recognition 20 pattern over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

28. The method of fabricating a semiconductor device as defined in claim 27,

25 wherein the recognition pattern includes:

 a first pattern extending in the X-axis direction of the two-dimensional coordinate system established on a surface of

the substrate; and

 a second pattern extending in the Y-axis direction; and
 wherein positioning of the semiconductor chip and the
 substrate is carried out by using the recognition pattern.

5

29. The method of fabricating a semiconductor device as
defined in any one of claims 20 to 26,
 wherein the conductive members are a plurality of layered
bumps.

10

30. The method of fabricating a semiconductor device as
defined in claim 29,

 wherein the bumps are formed by:
 a first step of bonding a first conductive wire to one
 of the electrodes of the semiconductor chip and cutting the
 bonded first conductive wire with part of the first conductive
 wire to remain on one of the electrodes;
 a second step of forming a first bump by pressing the
 remaining part of the first conductive wire on the electrode;
20 a third step of bonding a second conductive wire to the
 first bump and cutting the bonded second conductive wire with
 part of the second conductive wire to remain on the first bump;
 and
 a fourth step of forming a second bump by pressing the
25 remaining part of the second conductive wire on the first bump.

31. The method of fabricating a semiconductor device as

defined in claim 30,

wherein the first step is repeated for the plurality of electrodes to provide each of the electrodes with part of the first conductive wire; and

5 wherein the remaining parts of the first conductive wires on the electrodes are simultaneously pressed to form the first bumps at a time in the second step.

32. The method of fabricating a semiconductor device as defined in claim 31,

wherein the third step is repeated to provide each of the first bumps with part of the second conductive wire; and

wherein the remaining parts of the second conductive wires on the electrodes are simultaneously pressed to form the second bumps at a time in the fourth step.

10
15

ABSTRACT

A semiconductor device comprising: a substrate (30) including a plurality of holes (36) and a surface over which an interconnecting pattern (32) is formed, part of the interconnecting pattern (32) being superposed over the holes (36); a semiconductor chip (10) including a plurality of electrodes (12) which are disposed over another surface of the substrate (30) to correspond to the holes (36); and conductive members provided within the holes (36) for electrically connecting the electrodes (12) to the interconnecting pattern (32).

1/10

FIG. 1A

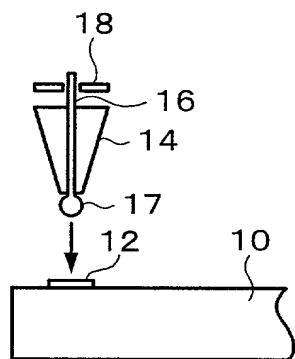


FIG. 1B

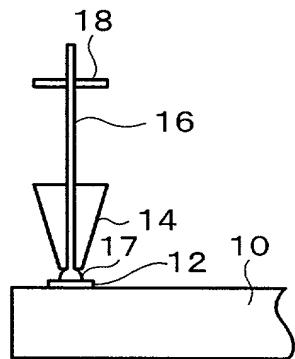
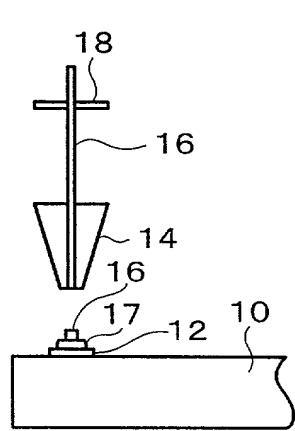


FIG. 1C



2/10

FIG. 2A

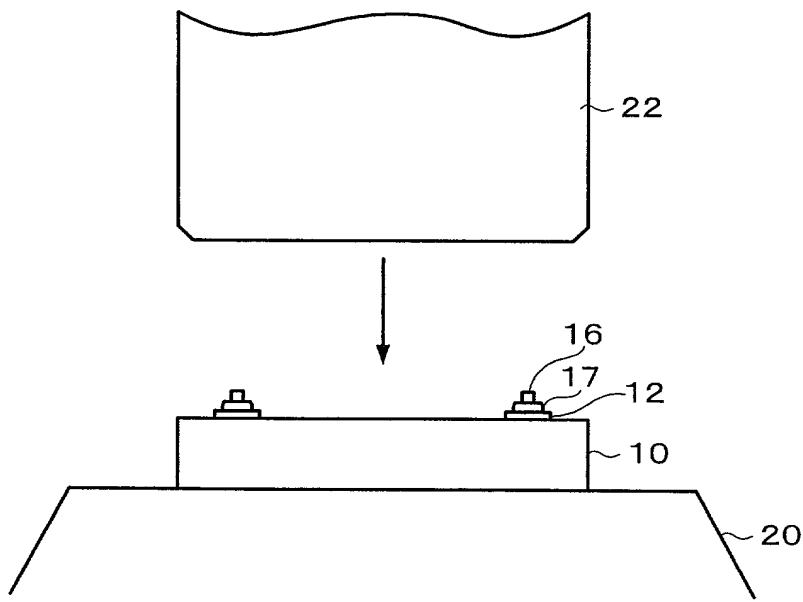
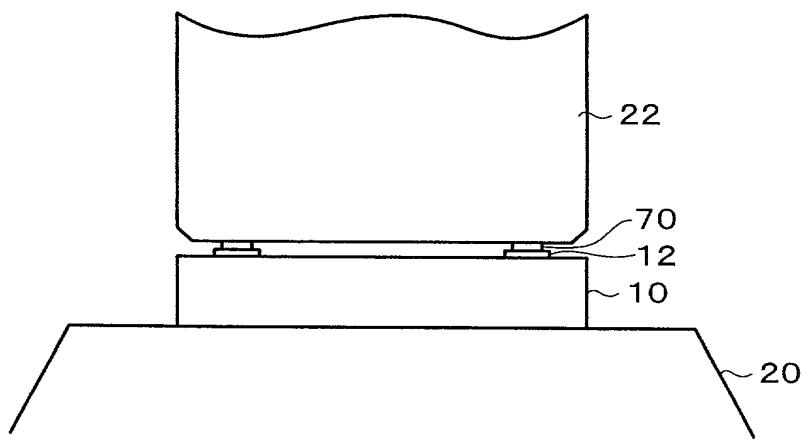


FIG. 2B



3/10

FIG. 3A

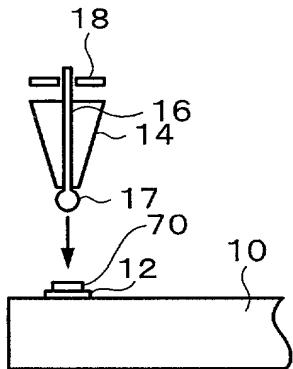


FIG. 3B

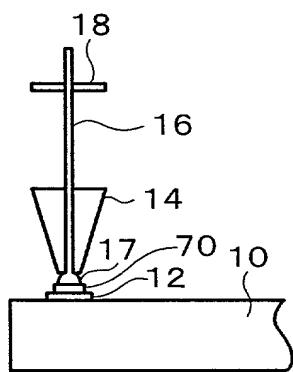
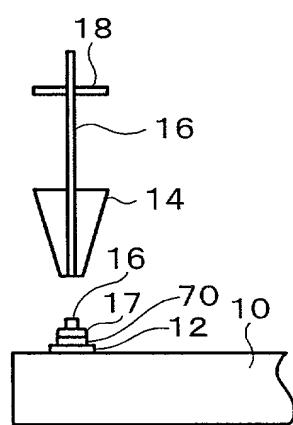


FIG. 3C



4/10

FIG. 4A

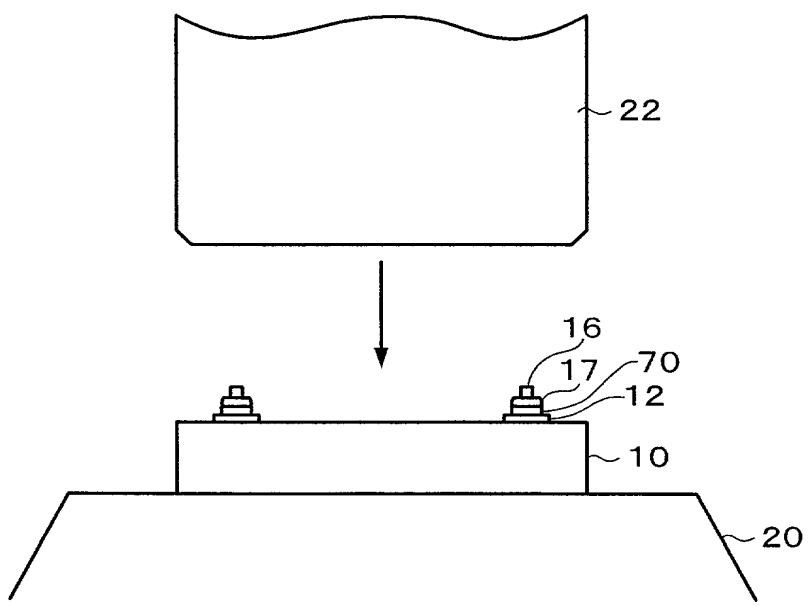
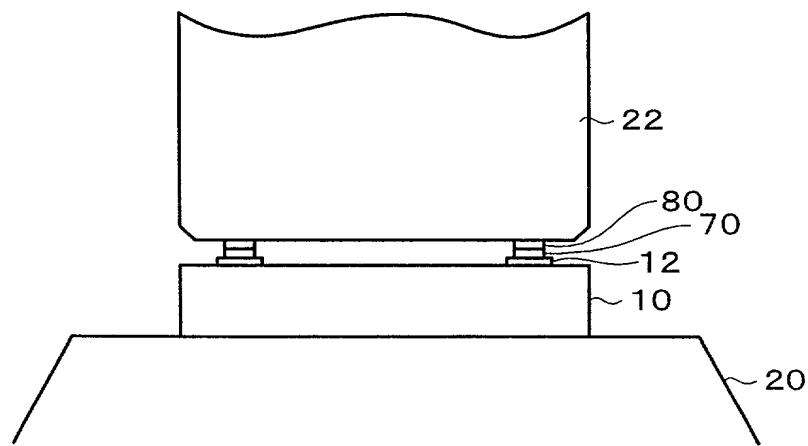


FIG. 4B



5/10

FIG. 5

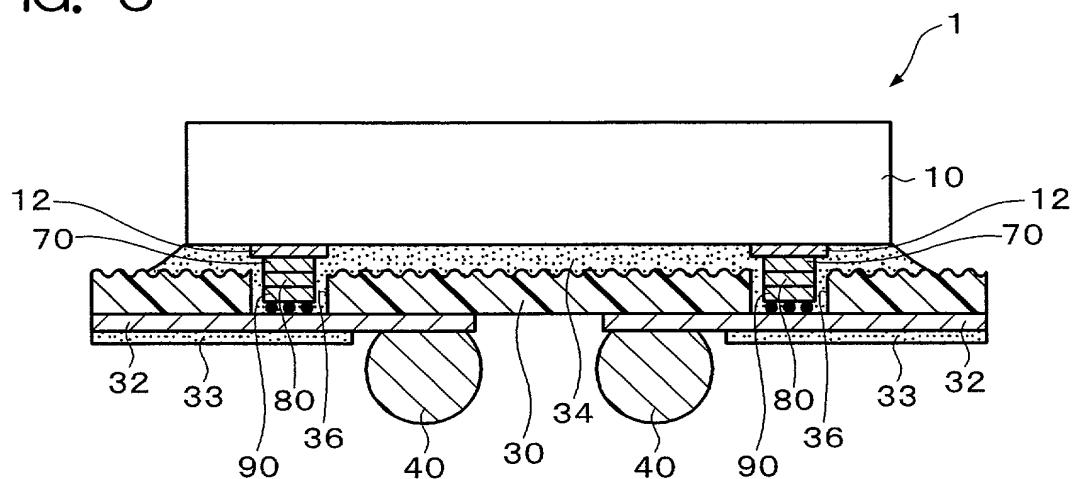
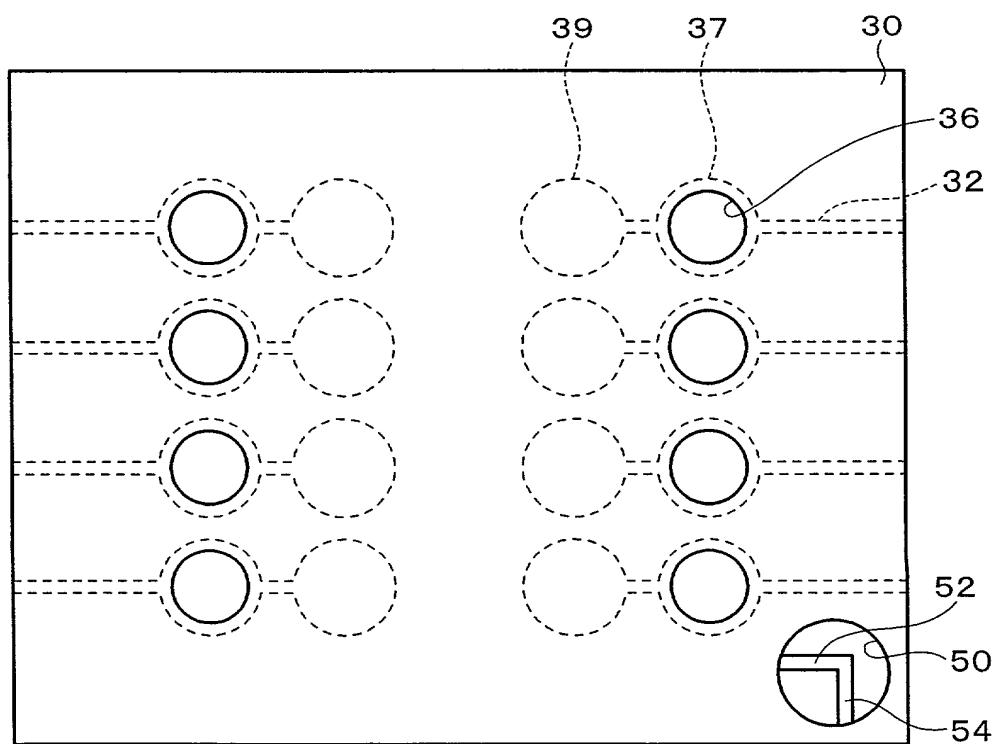
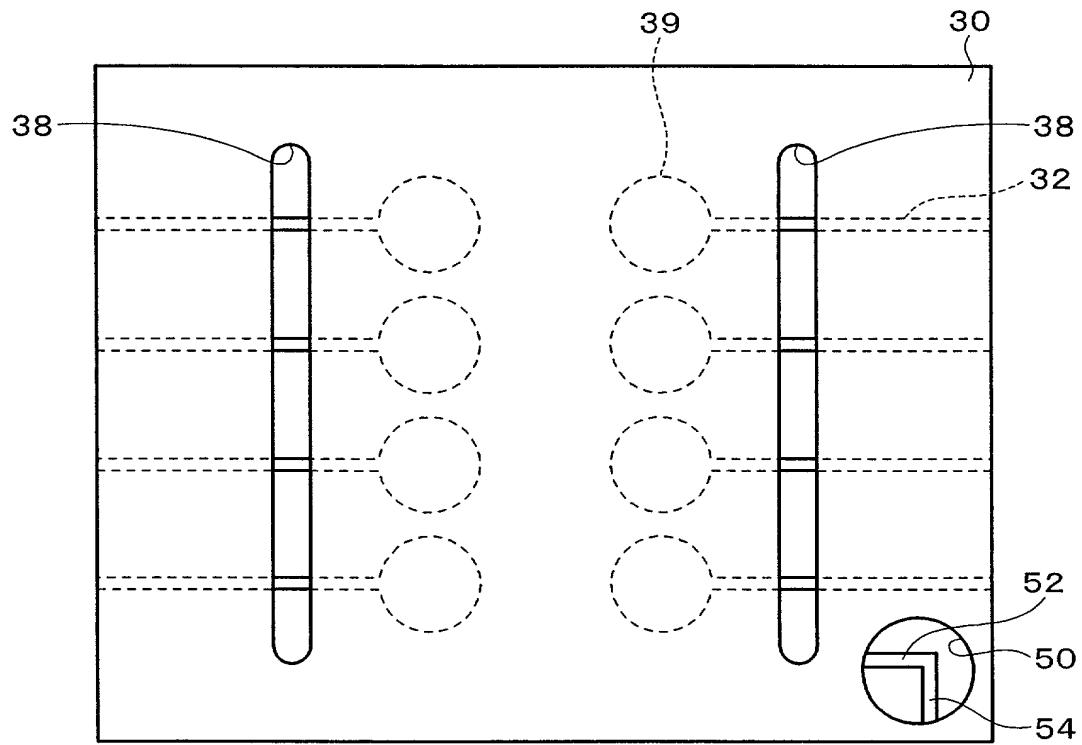


FIG. 6



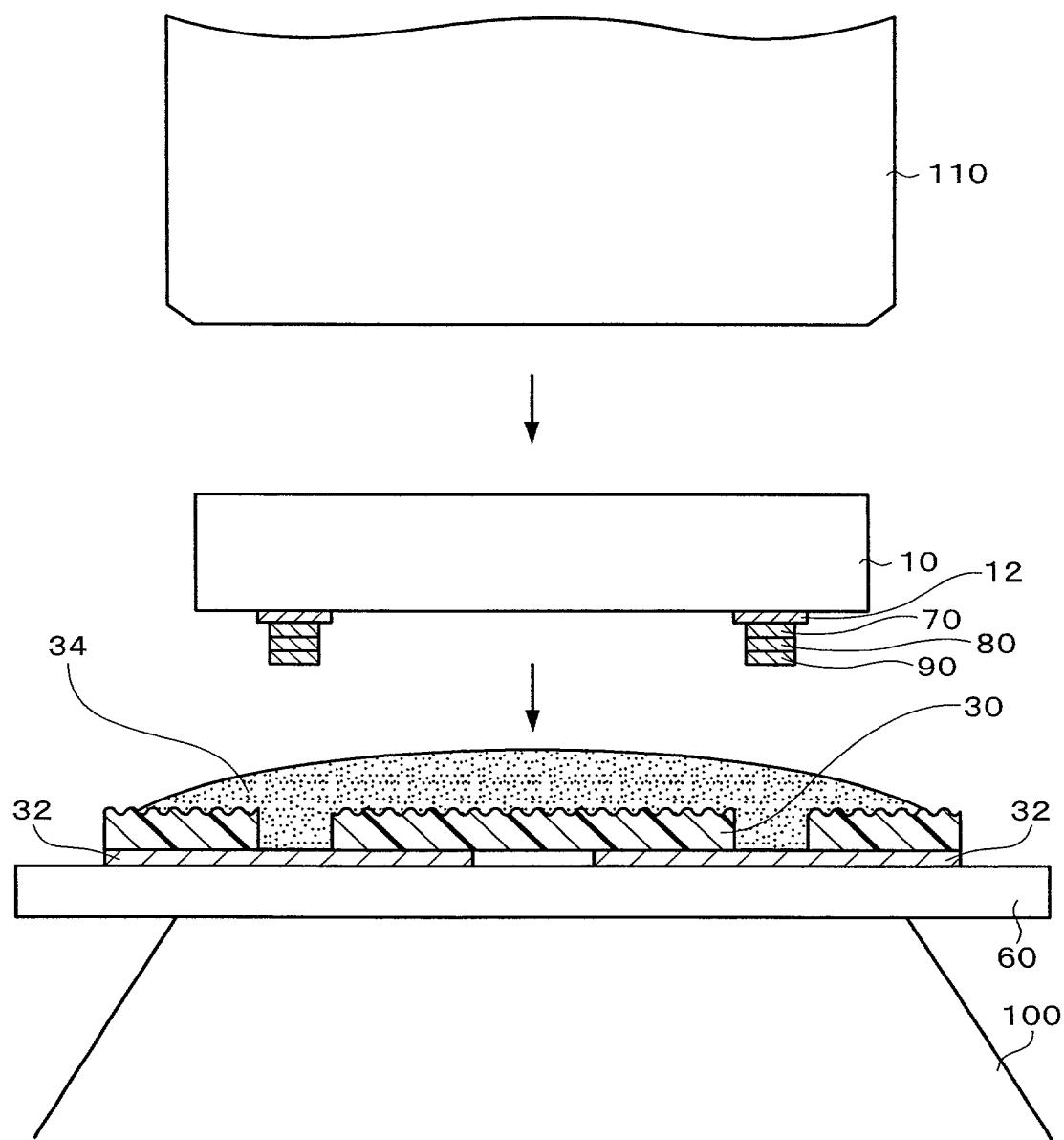
6/10

FIG. 7



7/10

FIG. 8



8/10

FIG. 9A

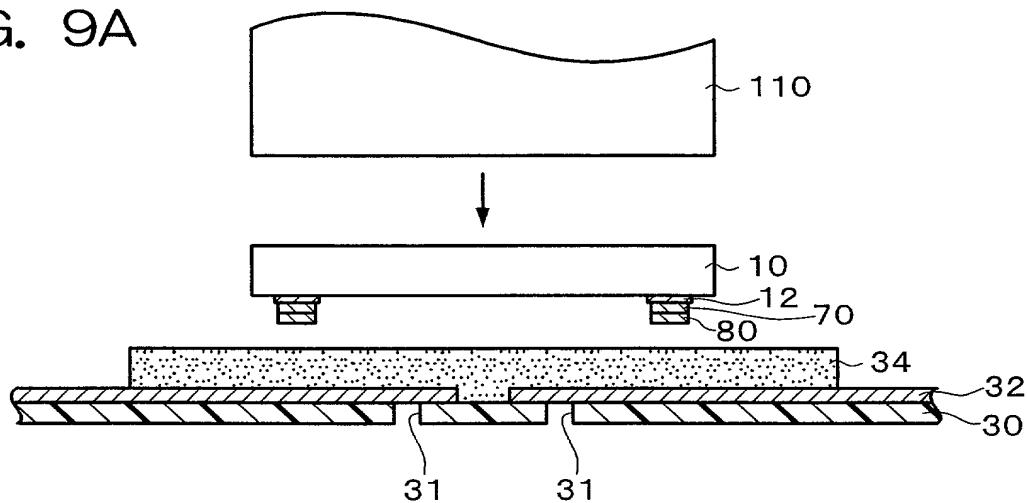


FIG. 9B

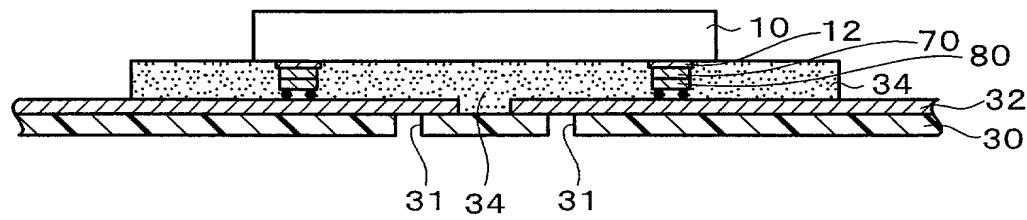


FIG. 9C

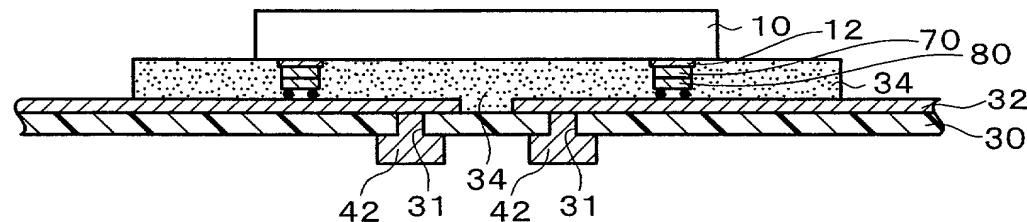
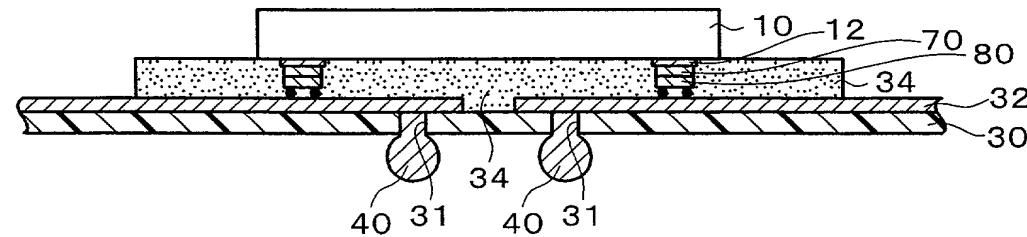
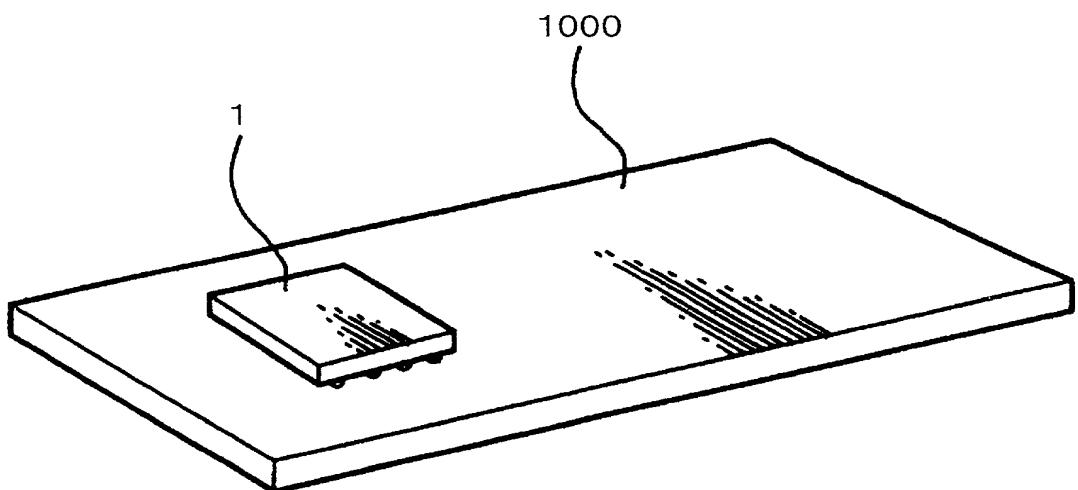


FIG. 9D



9/10

FIG. 10



10/10

FIG. 11

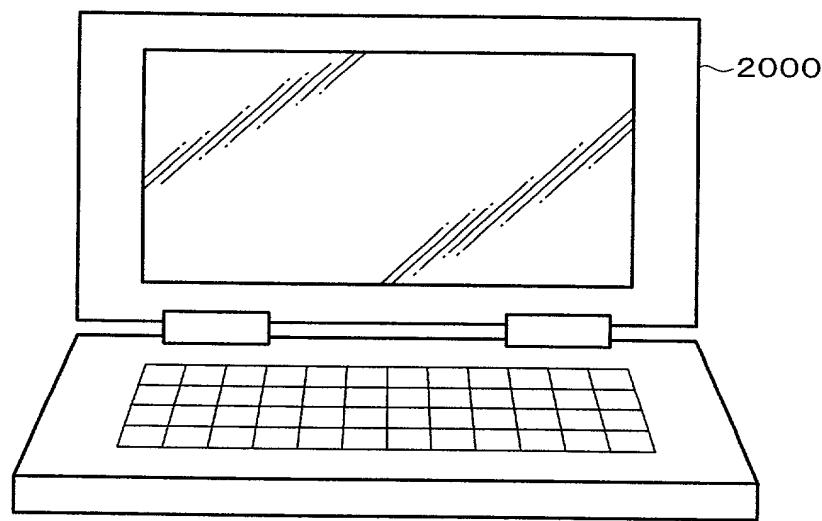
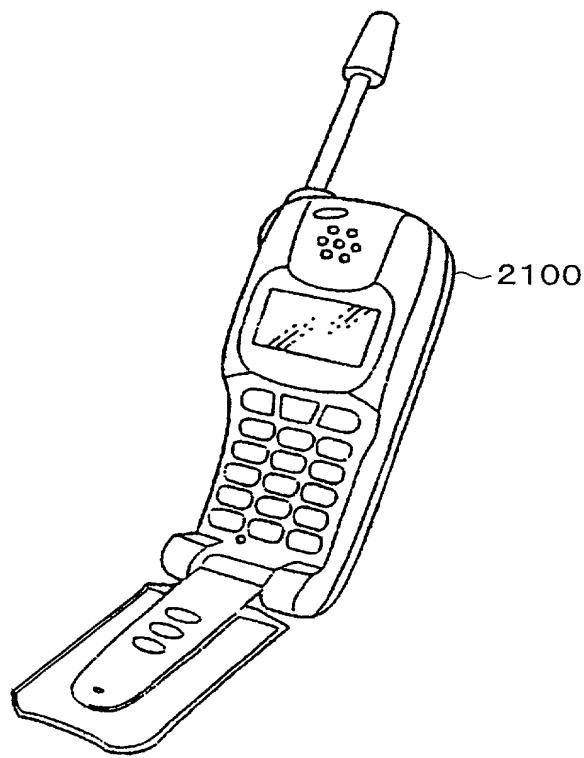


FIG. 12



Seiko Epson Ref. No.: F005224US00

Attorney's Ref. No.:

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

下記の名称の発明に関して請求範囲に記載され、特許出願してある発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

半導体装置及びその製造方法、回路基板並びに電子機器

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

に提出され、米国出願番号または
特許協定条約国際出願番号を _____ とし、
(該当する場合) _____ に訂正されました。

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

the specification of which is attached hereto unless the following box is checked:

was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration

(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基き下記の、米国以外の国の少なくとも1ヶ国を指定している特許協力条約365条(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

外国での先行出願

11-282474(P)

(Number)
(番号)

Japan

(Country)
(国名)

04/October/1999

(Day/Month/Year Filed)
(出願年月日)Priority Not Claimed
優先権主張なし(Number)
(番号)(Country)
(国名)(Day/Month/Year Filed)
(出願年月日)

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.)
(出願番号)(Filing Date)
(出願日)

私は下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

PCT/JP00/06767

(Application No.)
(出願番号)

29/September/2000

(Filing Date)
(出願日)(Application No.)
(出願番号)(Filing Date)
(出願日)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

(Application No.)
(出願番号)(Filing Date)
(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application:

Pending

(Status: Patented, Pending, Abandoned)
(現況:特許許可済、係属中、放棄済)(Status: Patented, Pending, Abandoned)
(現況:特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

(日本語宣言書)

委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

James A. Oliff, (Reg. 27,075)
 William P. Berridge, (Reg. 30,024)
 Kirk M. Hudson, (Reg. 27,562)
 Thomas J. Pardini, (Reg. 30,411)
 Edward P. Walker, (Reg. 31,450)
 Robert A. Miller, (Reg. 32,771)
 Mario A. Costantino, (Reg. 33,565)
 Caroline D. Dennison, (Reg. 34,494)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

James A. Oliff, (Reg. 27,075)
 William P. Berridge, (Reg. 30,024)
 Kirk M. Hudson, (Reg. 27,562)
 Thomas J. Pardini, (Reg. 30,411)
 Edward P. Walker, (Reg. 31,450)
 Robert A. Miller, (Reg. 32,771)
 Mario A. Costantino, (Reg. 33,565)
 Caroline D. Dennison, (Reg. 34,494)

書類送付先：
 OLIFF & BERRIDGE, PLC
 P.O. Box 19928
 Alexandria, Virginia 22320

Send Correspondence to:
 OLIFF & BERRIDGE, PLC
 P.O. Box 19928
 Alexandria, Virginia 22320

直接電話連絡先：（名前及び電話番号）
 OLIFF & BERRIDGE, PLC
 (703) 836-6400

Direct Telephone Calls to: (name and telephone number)
 OLIFF & BERRIDGE, PLC
 (703) 836-6400

唯一または第一発明者名
 橋 元 伸 晃

Full name of sole or first inventor
 Nobuaki HASHIMOTO

発明者の署名
 橋 元 伸 晃

日付

2001年 5月 14日

Inventor's signature

Date

May 14, 2001

住所
 日本国、長野県、諏訪市

Residence

Suwa-shi, Nagano-ken, Japan

国籍
 日本

Citizenship

Japan

私書箱
 392-8502 日本国長野県諏訪市大和3丁目3番5号
 セイコーエプソン株式会社内

Post Office Address

c/o Seiko Epson Corporation

3-5, Owa 3-chome, Suwa-shi, Nagano-ken 392-8502 Japan

第二共同発明者

Full name of second joint inventor, if any

第二共同発明者の署名

日付

Second inventor's signature

Date

住所
 日本国、_____

Residence

_____, _____, Japan

国籍

Citizenship

私書箱

Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）
 (Supply similar information and signature for third and subsequent joint inventors.)